IN THE SPECIFICATION

Please replace the paragraph beginning on page 12, line 4 with the following rewritten paragraph:

According to the present invention, two additional new fields are added to the queue link node for solving prior art problems of ~~memory jam and data lost~~ memory congestion and data loss due to errors caused by different frequencies of the MAC unit 114 of the switch 100 and the MAC unit 103 of the switch 102. As shown in FIG. 4B, according to the preferred embodiment of the present invention, in addition to the three conventional fields, the queue link node of the present invention further includes an IPG subtract count field and a port speed field. The contents of the two new additional fields are described as follows.

Please replace the paragraph beginning on page 13, line 4 with the following rewritten paragraph:

When a packet is transmitted to the RMAC unit 304, the counter 314 counts the clock cycle value corresponding to an IPG between the current packet and the previous packet. Then, the counted clock cycle value are subtracted by the clock cycle value corresponding to the 96 bit time and the result is recorded in the IPG subtract count field. When the packet is transmitted the TMAC unit 316, an IPG corresponding to the clock cycle value recorded in the IPG subtract count field is used as the IPG of the current packet and the next packet. The next packet is transmitted after the IPG passes when the TMAC

unit 316 transmits the current packet. Therefore, ~~memory jam~~ memory congestion or ~~data lost~~ data loss that has occurred in the conventional method can be avoided.

Please replace the paragraph beginning on page 16, line 12 with the following rewritten paragraph:

The packets P1, P2, P3, P4, P5 and P6 are transmitted out of the TMAC unit 316 after being processed by the switch 300. As shown in FIG. 7, in an output signal (c), when the packet P1 is transmitted, the packet P2 is transmitted after 96 bit time have elapsed. At this time, the IPG(1,2) obtained from the queue link node QLN(2) corresponding to the packet P2 is 94 bit time. Therefore, the TMAC unit 312 transmits the packet P3 after 94 bit time have elapsed. Similarly, because the calculated IPG(2,3), IPG(3,4) and IPG(4,5) are 92, 94, 92 bit time respectively, therefore, after the packet P3 is transmitted, the packets P4, P5 and P6 are sequentially transmitted with respective 92, 94, 92 bit time gaps. As shown in FIG. 7, the sum of all the IPGs of the adjacent packets of the packets P1, P2, ...,P5 in the input signal (c) is equal to the sum of all the IPGs for the packets ~~P1, P2,...,P5~~ P2, P3, ..., P6 in the output signal (c). Namely, when the input and the output speed of the switch for the packets are equal, the method is effective and efficient. As a result, ~~no jam~~ no congestion occurs in the memory 308 and therefore the transmission speed for the packets increases.